CLAIMS

What is claimed is:

1. A method of discharging a charge storage location of a transistor, the method comprising:

applying a first voltage to a control gate of a transistor, the control gate having at least a portion located adjacent to a select gate of the transistor, wherein the transistor includes a charge storage location including nanoclusters disposed within dielectric material of a structure of the transistor located below the control gate; and

applying a second voltage to a well region located below the control gate, wherein the applying the first voltage and the applying the second voltage generates a voltage differential across the structure for discharging electrons from the nanoclusters of the charge storage location.

2. The method of claim 2, wherein the nanoclusters of the charge storage location includes nanocrystals.

3. The method of claim 1, wherein the transistor includes a dielectric material located between the control gate and the select gate.

4. The method of claim 3, wherein the transistor further includes nanoclusters disposed within the dielectric material located between the control gate and the select gate.

5. The method of claim 1, further comprising:

applying the second voltage to a current terminal region concurrently with the applying the second voltage to the well region.

6. The method of claim 1, further comprising:

applying a third voltage to the select gate concurrently with the applying the first voltage to the control gate, wherein the third voltage is approximately in a range from equal to the second voltage to equal to 0 volts.

7. The method of claim 1, wherein the transistor further includes a second control gate located on an opposite side of the select gate from the control gate, the transistor further includes a second charge storage location including nanoclusters disposed in dielectric material of a second structure of a transistor and includes dielectric material located between the second control gate and the select gate, wherein discharging a charge stored in the second charge storage location comprises:

applying a third voltage to the second control gate; and

applying a fourth voltage to a well region located below the second control gate, wherein the applying the third voltage and the applying the fourth voltage generates a voltage differential across the second structure for discharging electrons from the nanoclusters of the second charge storage location.

8. The method of claim 7, wherein the first voltage is equal to the third voltage and the second voltage is equal to the fourth voltage.

9. The method of claim 1, wherein the first voltage is greater than 0 volts and the second voltage is less than 0 volts.

10. The method of claim 1, wherein the applying the first voltage and the applying the second voltage is performed during a discharge process characterized as a Fowler-Nordheim tunneling discharge process.

11. A memory array including a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a control gate locate over a substrate;

a select gate located over the substrate, the control gate including at least a portion located adjacent to the select gate;

a charge storage location including nanoclusters disposed in dielectric material located between the control gate and the substrate;

dielectric material located between the control gate and select gate;

a first current terminal region in the substrate;

a second current terminal region in the substrate; and

a channel region in the substrate located between the first current terminal region and the second current terminal region, wherein the control gate is located over at least a first portion of the channel region and the select gate is located over at least a second portion of the channel region.

12. The memory array of claim 11, wherein the transistor of each memory cell of the plurality further comprises:

a second control gate located over the substrate on an opposite side of the select gate from the control gate;

a second charge storage location including nanoclusters disposed in dielectric material located between the second control gate and the substrate; and

dielectric material located between the second control gate and the select gate, wherein the second control gate is located over at least a third portion of the channel region.

13. The memory array of claim 11, wherein the transistor of each memory cell of the plurality further comprises:

nanoclusters disposed in the dielectric material located between the control gate and the select gate.

14. The memory array of claim 11, wherein for the transistor of each memory cell of the plurality, the nanoclusters of the charge storage location includes nanocrystals.

15. The memory array of claim 11, wherein the memory cells of the plurality are arranged in rows and columns, the memory array further comprising:

a first plurality of word lines, wherein each word line of the first plurality is coupled to the control gate of the transistor of each memory cell of a plurality of memory cells located in a column of the array; and

a second plurality of word lines, wherein each word line of the second plurality is coupled to the select gate of the transistor of each memory cell of a plurality of memory cells located in a column of the array.

16. The memory array of claim 15, further comprising:

a plurality of bit lines, wherein each bit line of the plurality is coupled to a current terminal region of the transistor of each memory cell of a plurality of memory cells located in a row of the array.

17. The memory array of claim 11, wherein the transistor of each memory cell further includes a second control gate located over the substrate on an opposite side of the select gate from the control gate and further includes a second charge storage location including nanoclusters disposed in dielectric material located between the second control gate and the substrate, the memory array further comprising:

a third plurality of word lines, wherein each word line of the third plurality is coupled to the second control gate of the transistor of each memory cell of a plurality of memory cells located in a column of the array.

18. The memory array of claim 11, wherein for the transistor of each memory cell of the plurality, and the first portion of the channel region has a lower threshold voltage than a threshold voltage of the second portion of the channel region.

19. The memory array of claim 11, wherein for the transistor of each memory cell of the plurality, the first portion of the channel includes dopant characterized as having a low diffusion characteristic, and wherein the second portion is substantially void of the dopant.

20. The apparatus of claim 19, wherein the dopant includes at least one of antimony and arsenic.

21. The memory array of claim 11, further comprising:

a well region in the substrate, the well region being oppositely doped with respect to the first current terminal and the second current terminal region of the transistor of each memory cell of the plurality, wherein for the transistor of each memory cell of the plurality, the charge storage location is discharged by applying a first voltage to the control gate and a second voltage to the well region to generate a voltage differential across the dielectric material located between the control gate and the well region for discharging electrons from the nanoclusters of the charge storage location.

22. A method of discharging charge storage locations of transistors of plurality of memory cells located in a row of a memory array, the method comprising:

applying a first voltage to a word line, wherein each memory cell of a plurality of memory cells located in a row of a memory array includes a transistor having a charge storage location including nanoclusters disposed in dielectric material located between a control gate of the transistor and a substrate, wherein the control gate of the transistor of each memory cell of the plurality is coupled to the word line and is located over the substrate, wherein at least a portion of the control gate of the transistor of each memory cell of the plurality is located adjacent to a select gate of the transistor with dielectric material located between the control gate and the select gate; and

applying a second voltage to a well region in the substrate, wherein for the transistor of each memory cell of the plurality, the applying the first voltage and the applying the second voltage generates a voltage differential across the dielectric material having the nanoclusters of the charge storage location disposed therein for discharging electrons from the nanoclusters of the charge storage location.

23. The method of claim 22, further comprising:

applying a third voltage to a second word line concurrently with applying the first voltage to the first word line, wherein the second word line is coupled to the select gate of the transistor of each memory cell of the plurality, wherein the third voltage is approximately in a range from equal to the second voltage to equal to 0 volts.

24. The method of claim 22, wherein the applying the first voltage and the applying the second voltage is performed during a discharge process characterized as a Fowler-Nordheim tunneling discharge process.

25. The method of claim 22, wherein the transistor of each memory cell of the plurality further includes a second control gate located on an opposite side of the select gate from the control gate, the transistor of each memory cell of the plurality further includes a second charge storage location including nanoclusters disposed in dielectric material located between the second control gate of the transistor and the substrate and includes dielectric material located between the second control gate and the select gate, wherein the second control gate of the transistor of each memory cell of the plurality is coupled to a second word line, wherein discharging a charge stored in the second charge storage location of the transistor of each memory cell of the plurality comprises:

applying a third voltage to the second word line; and

applying a fourth voltage to the well region in the substrate, wherein for the transistor of each memory cell of the plurality, the applying the third voltage and the applying the fourth voltage generates a voltage differential across the dielectric material having the nanoclusters of the second charge storage location disposed therein for discharging electrons from the nanoclusters of the second charge storage location.